We Claim:

1. An electronic component, comprising:

a chip stack including a first semiconductor chip and a second semiconductor chip;

a plurality of flat conductors, each one of said plurality of flat conductors including an inner section, a central section, a transitional section, and an outer section, said inner section of each one of said plurality of flat conductors and said central section of each one of said plurality of flat conductors configured between said first semiconductor chip and said second semiconductor chip;

a package;

a plurality of first bonding connections; and

a plurality of second bonding connections;

said first semiconductor chip having a plurality of bonding surfaces;

said second semiconductor chip having a plurality of bonding surfaces;

each one of said plurality of first bonding connections connecting one of said plurality of bonding surfaces on said first semiconductor chip to said inner section of one of said plurality of flat conductors; and

each one of said plurality of second bonding connections connecting one of said plurality of bonding surfaces on said second semiconductor chip to said transitional section of one of said plurality of flat conductors.

2. The electronic component according to claim 1, wherein:

one of said plurality of first bonding connections is connected to said inner section of a given one of said plurality of flat conductors; and

one of said plurality of second bonding connections is connected to said transitional section of said given one of said plurality of flat conductors.

3. The electronic component according to claim 1, wherein:

said plurality of bonding surfaces on said first semiconductor chip and said plurality of bonding surfaces on said second semiconductor chip are configured at mutually congruent positions.

4. The electronic component according to claim 1, wherein:

said first semiconductor chip includes a bonding channel and said second semiconductor chip includes a bonding channel congruently configured with respect to said bonding channel of said first semiconductor chip;

said plurality of bonding surfaces on said first semiconductor chip are configured in said bonding channel of said first semiconductor chip; and

said plurality of bonding surfaces on said first semiconductor chip are configured in said bonding channel of said first semiconductor chip.

5. The electronic component according to claim 1, further comprising:

a first interposer layer or interposer film configured on said first semiconductor chip; and

a second interposer layer or interposer film configured on said second semiconductor chip;

said plurality of bonding surfaces on said first semiconductor chip configured on said first interposer layer or interposer film configured on said first semiconductor chip; and

said plurality of bonding surfaces on said second semiconductor chip configured on said second interposer layer or interposer film configured on said second semiconductor chip.

6. The electronic component according to claim 1, wherein:

said first semiconductor chip includes an active upper face mounted on said central section of each one of said plurality of flat conductors; and

said second semiconductor chip includes a rear face mounted on said central section of each one of said plurality of flat conductors.

7. The electronic component according to claim 1, wherein:

said first semiconductor chip includes an active upper face;

said second semiconductor chip includes an active upper face;

said outer section of each one of said plurality of flat conductors has a z-shaped bend aligned such that said active upper face of said first semiconductor chip and said active upper face of said second semiconductor chip are aligned in a direction of the bend.

8. The electronic component according to claim 1, wherein:

said first semiconductor chip includes an active upper face;

said second semiconductor chip includes an active upper face;

said outer section of each one of said plurality of flat conductors has a z-shaped bend aligned such that said active upper face of said first semiconductor chip and said active upper face of said second semiconductor chip are aligned in a direction opposite the bend.

9. The electronic component according to claim 1, wherein:

said second semiconductor chip includes an active upper face; and

said transitional section of each one of said plurality of flat conductors has a bend toward said active upper face of said second semiconductor chip.

10. A method for producing an electronic component, the method which comprises:

providing a first semiconductor chip having a plurality of bonding surfaces and a second semiconductor chip having a plurality of bonding surfaces configured congruently with respect to the plurality of bonding surfaces of the first semiconductor chip, the first semiconductor chip and the second semiconductor chip being for a chip stack;

aligning and fitting the first semiconductor chip in a component position of a flat conductor frame by mounting an active upper face of the first semiconductor chip on one face of a central section of each one of a plurality of flat conductors and producing a plurality of first bonding connections between the plurality of bonding surfaces of the first semiconductor chip and corresponding inner sections of the plurality of the flat conductors;

mounting a rear face of the second semiconductor chip on an opposite face of the central section of each one of the plurality of flat conductors and producing a plurality of second bonding connections between the plurality of bonding surfaces of the second semiconductor chip and corresponding

transitional sections of the plurality of the flat conductors; and

packaging a chip stack formed by the first semiconductor chip, the second semiconductor chip, the plurality of first bonding connections, the plurality of second bonding connections, and the plurality of flat conductors in a plastic encapsulation compound, leaving outer sections of the flat conductors of the flat conductor frame projecting.

11. The method according to claim 10, which further comprises:

after the chip stack has been packaged, stamping out the component position from the flat conductor frame, and bending the outer section of the plurality of flat conductors.

12. The method according to claim 10, which further comprises:

fitting an interposer film having a central bonding channel to the active upper face of the first semiconductor chip and to an active upper face of the second semiconductor chip; and

producing additional bonding connections from the interposer film to contact surfaces in the central bonding channel.